We Claim:

1. A method for reducing a number of addresses to be stored and further processed when memory cells of a memory array are checked, the method which comprises:

further processing an address of a memory cell having been detected as faulty during a test method, as a first fault address;

comparing the first fault address, in a first comparison process, with a second fault address, the second fault address constituting an address of at least one of a word line and a bit line to be completely repaired;

neither storing nor further processing the first fault address, if the first fault address corresponds to the second fault address; and

storing the first fault address, if the first fault address and the second fault address do not correspond.

2. The method according to claim 1, which comprises:

checking, in a second comparison process, whether more than a given number of first fault addresses of at least one of a bit

line and a word line is stored for at least one of a word line and a bit line;

detecting an address of the at least one of the word line and the bit line for which more than the given number of first fault addresses is stored, as a further new second fault address; and

taking the further new second fault address into account in subsequent first comparison processes.

3. The method according to claim 1, which comprises:

checking, in a second comparison process, whether more than a given number of first fault addresses of at least one of a bit line and a word line is stored for at least one of a word line section and a bit line section;

detecting an address of the at least one of the word line section and the bit line section for which more than the given number of first fault addresses is stored, as a further new second fault address; and

taking the further new second fault address into account in subsequent first comparison processes.

4. The method according to claim 1, which comprises using a complete address of a faulty memory cell as a first fault address.

5. The method according to claim 2, which comprises providing different numbers for the given number of the first fault addresses of the at least one of the word line and the bit line.

6. The method according to claim 3, which comprises providing different numbers for the given number of the first fault addresses of the at least one of the word line section and the bit line section.

7. The method according to claim 1, which comprises using an address for a plurality of at least one of bit lines and word lines provided in one of a word line block and a bit line block, the one of the word line block and the bit line block being completely replaced in case of a repair, as at least one of the first fault address and the second fault address.

8. A device for reducing a number of addresses of faulty memory cells, comprising:

an arithmetic unit having a memory including word lines, bit lines and memory cells with respective addresses;

said arithmetic unit further processing, as first fault addresses, the addresses of given ones of said memory cells having been detected as faulty in a test;

said arithmetic unit comparing the first fault addresses with second fault addresses in a first comparison process, the second fault addresses constituting addresses of given ones of said word lines and said bit lines which are to be completely repaired; and

said arithmetic unit not storing a respective one of the first fault addresses, if the respective one of the first fault addresses corresponds to a respective one of the second fault addresses, and said arithmetic unit storing the respective one of the first fault addresses, if the respective one of the first fault addresses does not correspond to the respective one of the second fault addresses.

9. The device according to claim 8, wherein said arithmetic unit checks, in a second comparison process, whether more than a given number of the first fault addresses of one of said bit lines and said word lines is stored for one of a word line and a bit line, said arithmetic unit storing, as a new further second fault address, an address of the one of the word line and the bit line for which more than the given number of first

fault addresses are stored and taking the new further second fault address into account in subsequent first comparison processes.

10. The device according to claim 8, wherein:

said arithmetic unit has a first comparison unit, said first comparison unit has a first row of serially connected registers and a second row of serially connected registers, each of said registers in said first row is assigned to a respective one of said registers in said second row;

said first comparison unit has a clock input for receiving a clock signal;

a first one of said registers in said first row is configured to be supplied with a first fault address, said first row of serially connected registers is configured such that the first fault address is shifted forward by a respective one of said registers in said first row at each clock signal; and

said first comparison unit comparing, between clock signals, in each case the addresses of assigned ones of said registers of said first row and said second row and deleting an address of one of said registers of said first row, if the addresses

of said assigned ones of said registers of said first row and said second row correspond.

11. The device according to claim 8, wherein:

said arithmetic unit has a second comparison unit, said second comparison unit has a third row of serially connected registers and a fourth row of serially connected registers, each of said registers in said third row is assigned to a respective one of said registers in said fourth row;

said second comparison unit has a clock input for receiving a clock signal;

a first one of said registers in said fourth row is configured to be supplied with a first fault address after the clock signal;

said fourth row of serially connected registers is configured such that the first fault address is shifted forward by a respective one of said registers in said third row at each clock signal;

said second comparison unit comparing, between clock signals, in each case the addresses of assigned ones of said registers of said third row and said fourth row and deleting an address

of one of said registers of said fourth row, if the addresses of said assigned ones of said registers of said third row and said fourth row correspond;

said second comparison unit reading an address of one of said registers of said fourth row into an assigned one of said registers of said third row if said assigned one of said registers of said third row is detected as being empty during a comparison;

said second comparison unit serially reading into said first row and processing, in a given operation, the first fault addresses of at least one of a word line and a bit line, said second comparison unit checking, after performing the given operation, whether more than a given number of said serially connected registers of said third row is occupied; and

said arithmetic unit writing an address of one of a checked one of said word lines and a checked one of said bit lines into a free one of said serially connected registers of said second row as a further new second fault address.